WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a semiconductor substrate; and

a compliant interconnect element disposed on a first surface of the substrate, said compliant interconnect element defining a chamber between the first surface of the substrate and a surface of the interconnect element.

2. The structure of claim **1**, wherein the interconnect element comprises a compliant layer.

3. The structure of claim **2**, wherein the compliant layer comprises a polymer.

4. The structure of claim **3**, wherein the polymer comprises silicone.

5. The structure of claim **2**, wherein the chamber is surrounded on all of its sides by the compliant layer and the first surface of the chip.

6. The structure of claim **1**, wherein the chamber has a height within the range of about 50 μm to about 200 μm.

7. The structure of claim **2**, wherein the compliant layer has a thickness within the range of about 5 μm to about 500 μm.

8. The structure of claim **1**, wherein the substrate comprises a device.

9. The structure of claim **8**, wherein the device comprises an integrated circuit.

10. The structure of claim **9**, wherein the device comprises a micro-electro mechanical system.

11. The structure of claim **1**, further comprising:

an encapsulation layer disposed on a second surface of the semiconductor substrate.

12. The structure of claim **1**, further comprising:

a first conducting pad on the substrate; and

a conducting layer, disposed on the compliant interconnect element in contact with the first conducting pad.

13. The structure of claim **12**, wherein the conducting layer comprises metal.

14. The structure of claim **13**, wherein the metal is selected from the group consisting of titanium, copper, nickel, and gold.

15. The structure of claim **13**, wherein the conducting layer has a thickness within the range of about 2 μm to about 5 μm.

16. The structure of claim **12**, further comprising:

a plurality of conducting pads on the substrate,

wherein the conductive layer comprises a plurality of lines, each of the lines contacting one of the plurality of conducting pads, the lines defining a pad redistribution pattern.

17. The structure of claim **12**, further comprising:

a printed circuit board having a second conducting pad disposed thereon,

wherein the second conducting pad is in electrical communication with the first conducting pad on the substrate via the conducting layer.

18. A method for forming a semiconductor structure, said method comprising:

providing a semiconductor substrate; and

providing a compliant interconnect element on a first surface of the substrate, said compliant interconnect element defining a chamber between the compliant interconnect element and the first surface of the substrate.

19. The method of claim **18**, wherein providing the compliant interconnect element comprises providing a compliant layer.

20. The method of claim **19**, wherein providing the compliant layer comprises providing a transfer substrate having a compliant layer disposed thereon.

21. The method of claim **20**, wherein providing a transfer substrate comprises providing a glass substrate.

22. The method of claim **18**, wherein providing a semiconductor substrate comprises a providing a plurality of singulated dies, each of said die including a semiconductor device.

23. The method of claim **22**, further comprising:

encapsulating each one of the plurality of singulated dies in a protective material to form a reconstituted wafer.